ABSTRACT

In processing an instruction request, the invention determines whether the request is speculative or not based upon a bit field within the instruction. If the request is speculative, bus congestion and/or target memory is assessed for conditions and a decision is made, based on the conditions, as to whether or not to process the request. To facilitate the invention, certain bit fields within the instruction are encoded to identify the request as speculative or not. Additional bit fields may define a priority of a speculative request to influence the decision to process as based on the conditions. CPU architectures incorporating prefetch logic may be modified to recognize instructions encoded with speculation and priority identification fields to implement the invention in existing systems. Other logic, e.g., bus controllers and switches, may similarly process speculative requests to enhance system performance.